

IN THE CLAIMS:

Please cancel claim 37.

Please amend the claims as follows:

- 1 1. (CURRENTLY AMENDED) Apparatus for enabling an instruction to control data flow
2 bypassing hardware within a processor of a programmable processing engine, the apparatus
3 comprising:
4 a pipeline of the processor, the pipeline having a plurality of stages including instruction
5 decode, writeback, and execution stages, the execution stage having a plurality of parallel
6 execution units; and
7 an instruction set of the processor, the instruction set defining a first register decode
8 value, ~~that specifies one of a first register decode value which~~ that defines source operand
9 bypassing ~~that allows source operand data to be shared among the plurality of execution units,~~
10 and a second register decode value that defines result bypassing ~~that allows bypassing of a result~~
11 from a previous instruction executing in pipeline stages of the processor.
- 1 2. (ORIGINAL) The apparatus of Claim 1 further comprising:
2 a register file containing a plurality of general-purpose registers for storing intermediate
3 result data processed by the execution units; and
4 a memory for storing one or transient data unique to a specific process and pointers
5 referencing data structures.
- 1 3. (CURRENTLY AMENDED) The apparatus of Claim 1 wherein the second register decode
2 value comprises:
3 one of a result bypass (RRB) operand and an inter-unit result bypass (RIRB) operand,
4 each of which explicitly controls data flow within the pipeline of the processor.

1 4. (ORIGINAL) The apparatus of Claim 3 wherein the execution units comprise a current
2 execution unit and an alternate execution unit, and wherein the RRB operand denotes the current
3 execution unit and the RIRB operand denotes the alternate execution unit.

1 5. (ORIGINAL) The apparatus of Claim 3 wherein the RRB operand explicitly infers feedback
2 of the data delivered from a current one of the execution units to an input register of the current
3 execution unit over a feedback path.

1 6. (ORIGINAL) The apparatus of Claim 5 wherein the writeback stage comprises an interstage
2 register and wherein the RRB operand enables bypassing write-back of the data processed by the
3 execution units to one of the register file or the interstage register of the writeback stage.

1 7. (CURRENTLY AMENDED) The apparatus of Claim 2 wherein the first register decode
2 value comprises a source bypass (RISB) operand that allows source operand data to be shared
3 among the parallel execution units of the pipelined processor.

1 8. (ORIGINAL) The apparatus of Claim 7 wherein the execution units comprise a main
2 execution unit and a secondary execution unit, and wherein the RISB operand allows the
3 secondary execution unit to receive data stored at an effective memory address specified by a
4 displacement operand in the previous instruction executed by the main execution unit.

1 9. (CURRENTLY AMENDED) A method for enabling an instruction to control data flow
2 bypassing hardware within a pipelined processor of a programmable processing engine, the
3 method comprising the steps of:

4 defining a first register decode value that specifies ~~one of a first register decode value~~
5 ~~which defines source operand bypassing of source operand data~~ and a second register decode
6 value that defines result bypassing ~~of a result~~ from a previous instruction executing in pipeline
7 stages of the processor; and

8 identifying a pipeline stage register for use as a source operand in an instruction
9 containing the first or the second register decode value.

1 10. (CURRENTLY AMENDED) The method of Claim 9 further comprising: ~~the step of~~
2 explicitly controlling data flow within the pipeline stages of the processor through the use
3 of a register result bypass (RRB) operand in said second register decode value.

1 11. (PREVIOUSLY PRESENTED) The method of Claim 10 further comprising:
2 including pipeline stages having instruction decode, writeback and execution stages, and
3 wherein the execution stage has multiple parallel execution units including a current execution
4 unit and an alternate execution unit.

1 12. (CURRENTLY AMENDED) The method of Claim 11 wherein the step of explicitly
2 controlling comprises ~~the steps of:~~
3 retrieving data from the current execution unit; and
4 returning the data to an input execution register specified by the RRB operand, thereby
5 bypassing write-back of the data to either a register file or memory at the writeback stage.

1 13. (CURRENTLY AMENDED) The method of Claim 12 wherein the step of identifying
2 further comprises ~~the steps of:~~
3 explicitly specifying the pipeline stage register to be used as the source operand for the
4 instruction.

1 14. (PREVIOUSLY PRESENTED) The method of Claim 13 further comprising:
2 encoding the RRB operand in fewer bits than a regular register operand.

1 15. (PREVIOUSLY PRESENTED) The method of Claim 9 further comprising:

2 including pipeline stages having instruction decode, writeback and execution stages, and
3 wherein the execution stage has multiple parallel execution units including a current execution
4 unit and an alternate unit; and

5 sharing source operand data among the parallel execution units of the pipelined processor
6 through the use of a source bypass (RISB) operand in said first register decode value.

1 16. (CURRENTLY AMENDED) The method of Claim 15 wherein the step of sharing further
2 comprises: the step of

3 receiving data at the alternate execution unit, the data stored at a memory address
4 specified by a displacement operand in a previous instruction executed by the current execution
5 unit of the processor.

1 17. (CURRENTLY AMENDED) The method of Claim 16 wherein the step of sharing further
2 comprises: the step of

3 realizing two memory references through the use of a single bus operation over a local
4 bus.

1 18. (CURRENTLY AMENDED) The method of Claim 17 wherein the step of sharing further
2 comprises: the step of

3 encoding the RISB operand with substantially fewer bits than those needed for a
4 displacement address.

1 19. (CURRENTLY AMENDED) A computer readable medium containing executable program
2 instructions for enabling an instruction to control data flow bypassing hardware within a
3 pipelined processor of a programmable processing engine, the executable program instructions
4 comprising program instructions for:

5 defining a first register decode value that specifies one of a first register decode value that
6 defines source operand bypassing of source operand data and a second register decode value that

7 defines result bypassing of a result from a previous instruction executing in pipeline stages of the
8 processor; and

9 identifying a pipeline stage register for use as a source operand in a current instruction
10 containing the register decode value.

1 F1 20. (ORIGINAL) The computer readable medium of Claim 19 further comprising program
2 instructions for explicitly controlling data flow within the pipeline stages of the processor
3 through use of a register result bypass operand.

1 21. (ORIGINAL) The computer readable medium of Claim 20 further comprising program
2 instructions for sharing source operand data among parallel execution units of the pipelined
3 processor through the use of a source bypass operand.

1 22. (CANCELLED)

1 23. (CANCELLED)

1 24. (CANCELLED)

1 25. (CANCELLED)

1 26. (CANCELLED)

1 27. (CANCELLED)

1 28. (PREVIOUSLY PRESENTED) A processor comprising:
2 a first execution unit having at least one first input and a first output;
3 at least one second execution unit having at least one second input and a second output;

4 a first input register connected to said at least one first input;
5 a second input register;
6 a multiplexer having a first input from said first input register, a second input from said
7 second input register, and an output to said at least one second execution unit; and
8 a register decode value that specifies bypassing data from said first input register to said
9 at least one second execution unit via said multiplexer.

1 29. (PREVIOUSLY PRESENTED) The processor of claim 28 further comprising:
2 a first instruction having at least one first source operand and a first destination, said first
3 execution unit processing said first instruction;
4 a second instruction having at least one second source operand and a second destination
5 operand, said at least one second source operand is the same as said at least one first source
6 operand; and
7 means for replacing said at least one second source operand with said register decode
8 value.

1 30. (PREVIOUSLY PRESENTED) The processor of claim 29 further comprising:
2 a register file connected to said first input register and said second input register; and
3 means for loading said at least one first and said at least one second source operands from
4 said register file.

1 31. (PREVIOUSLY PRESENTED) The processor of claim 29 further comprising:
2 a memory connected to said first input register; and
3 means for loading said at least one first and said at least one second source operands from
4 said memory.

1 32. (PREVIOUSLY PRESENTED) The processor of claim 29, said means for replacing further
2 comprising:
3 an instruction decode mechanism; and

4 means for said multiplexer choosing input from said first input register.

1 33. (PREVIOUSLY PRESENTED) The processor of claim 29 further comprising:
2 said register decode value having fewer bits than said at least one second source operand.

1 34. (PREVIOUSLY PRESENTED) The processor of claim 29 further comprising:
2 a displacement value within said at least one first and said at least one second source
3 operands, said displacement value specifying an effective memory address where data is stored.

1 35. (PREVIOUSLY PRESENTED) The processor of claim 29 further comprising:
2 a displacement value within said first destination operand, said displacement value
3 specifying an effective memory address where data is stored.

1 36. (PREVIOUSLY PRESENTED) Electromagnetic signals propagating over a computer
2 network comprising:
3 said electromagnetic signals carrying instruction for execution on a processor for
4 performing the method of claim 9.

1 37. (CANCELLED)

1 38. (PREVIOUSLY PRESENTED) The method of Claim 9 further comprising:
2 including pipeline stages having instruction decode, writeback and execution stages, and
3 wherein the execution stage has multiple parallel execution units including a current execution
4 unit and an alternate execution unit; and
5 explicitly controlling data flow within the pipeline stages of the processor through the use
6 of a register result bypass (RIRB) operand to bypass the writeback stage and to allow result data
7 from an alternate execution unit to flow directly to an input execution register.

1 39. (PREVIOUSLY PRESENTED) The apparatus of Claim 3 wherein the RIRB operand
2 explicitly infers feedback of the data delivered from an alternate one of the execution units to an
3 input register of the current execution unit over a feedback path.

1 40. (PREVIOUSLY PRESENTED) Apparatus for enabling an instruction to control data flow
2 within a processor of a programmable processing engine, the apparatus comprising:
3 a pipeline of the processor, the pipeline having a plurality of stages including instruction
4 decode, writeback and execution stages, the execution stage having a plurality of parallel
5 execution units;
6 a multiplexer connecting parallel execution units; and
7 an instruction set of the processor, the instruction set defining a register decode value that
8 controls said multiplexer to bypass a source operand from a previous instruction executing in
9 pipeline stages of the processor to the source operand of a current instruction.

1 41. (PREVIOUSLY PRESENTED) The apparatus of Claim 40 further comprising:
2 a register file containing a plurality of general-purpose registers for storing intermediate
3 result data processed by the execution units.

1 42. (PREVIOUSLY PRESENTED) The apparatus of Claim 40 further comprising:
2 a memory for storing one or transient data unique to a specific process and pointers
3 referencing data structures.

1 43. (PREVIOUSLY PRESENTED) The apparatus of Claim 40 wherein the register decode value
2 comprises:
3 a source bypass operand (RISB) that allows source operand data to be shared among the
4 parallel execution units of the pipelined processor.

1 44. (PREVIOUSLY PRESENTED) The apparatus of Claim 40 wherein the execution units
2 comprise:

3 a main execution unit and a secondary execution unit, wherein the RISB operand allows
4 the second execution unit to receive data stored at a memory address specified by a displacement
5 operand in the previous instruction executed by the main execution unit.

1 45. (PREVIOUSLY PRESENTED) The apparatus of Claim 44 wherein the instruction set of the
2 processor comprises:

3 an opcode directed to the main execution unit, said opcode having sufficient bits to
4 encode a displacement operand;
5 an opcode directed to the secondary execution unit; and
6 micro-opcodes to initiate memory prefetches without requiring a dedicated instruction.

1 46. (PREVIOUSLY PRESENTED) A method for enabling an instruction to control data flow
2 within a pipelined processor of a programmable processing engine, the method comprising the
3 steps of:

4 defining a register decode value that specifies one of source operand bypassing from a
5 previous instruction executing in pipeline stages of the processor; and
6 identifying a pipeline stage register for use as a source operand in an instruction
7 containing the register decode value.

1 47. (PREVIOUSLY PRESENTED) The method of Claim 46 further comprising:

2 including pipeline stages having instruction decode, writeback and execution stages, and
3 wherein the execution stage has multiple parallel execution units including a current execution
4 unit and an alternate execution unit.

1 48. (PREVIOUSLY PRESENTED) The method of claim 47 further comprising:

2 sharing source operand data among the parallel execution units of the pipelined processor
3 through the use of a source bypass (RISB) operand.

1 49. (PREVIOUSLY PRESENTED) The method of claim 48 further comprising:

2 receiving data at said alternate execution unit, the data stored at a memory address
3 specified by a displacement operand in a previous instruction executed by said current execution
4 unit of the processor.

1 F1 50. (PREVIOUSLY PRESENTED) The method of claim 49 further comprising:
2 realizing two memory references through the use of a single bus operation over a local
3 bus.

1 51. (PREVIOUSLY PRESENTED) The method of claim 49 further comprising:
2 encoding the RISB operand with substantially fewer bits than those needed for a
3 displacement address.

1 52. (CURRENTLY AMENDED) Electromagnetic signals propagating on a computer network,
2 comprising:
3 said electromagnetic signals carrying instruction for the practice of the method of ~~Claim~~
4 ~~9 or Claim 46.~~

1 53. (CURRENTLY AMENDED) A computer readable media comprising:
2 said computer readable media containing executable program instruction for the practice
3 of the method of ~~Claim 9 or Claim 46.~~